IEEE - Solid State Circuit Society

Italian Chapter

Distinguished Lecture Seminars

University of Milan- Bicocca

Dept. of Physics 'G. Occhialini'

Microelectronics Group

Seminar Announcement

September, 16th, 2016 – Friday

Building U2 – Room 01 – Piazza della Scienza, 3 – 20126 Milan (Italy)

Hideto Hidaka (CTO, Renesas Electronics)

Embedded Memory Technology, Applications and Prospects in Embedded Systems

➔ *h. 13.30 – 14.45* ➔

As new memory technologies evolve, new memory hierarchy is emerging for lower-power designs for expanding and distributed embedded systems. Embedded SRAM, DRAM, and Flash, major practical embedded memories in use, are analyzed in actual embedded applications and market size, technology prospects and sub-system developments are discussed. Insights into emerging/emerged non-volatile memories like MRAM and ReRAM are also provided with actual requirements by emerging markets at the IoT/IoE age.

1. Advantages of embedded memory re-visited
2. Impact of 2.5D/3D integrations for embedded systems
3. Economical / technological survey on the family of embedded memories
4. Meaning of non-volatility and programmability and its impact on the VLSI evolutions
5. Future prospects of embedded memory technology and applications

Hideto Hidaka earned the B.S., M.S., and Ph.D. degrees in electronic engineering from the University of Tokyo, Tokyo, Japan. In Mitsubishi Electric, Renesas Technology, and Renesas Electronics he has been engaged in the research and development of high-density, application-specific, and embedded aspects of DRAM technology and circuits, embedded-flash memory for MCU, embedded non-volatile memory technology, and related technology platforms and analog IPs for MCU and SOC products. Since 2005 he and his team have created the world's first split-gate embedded SONOS flash memory for MCU products at 90 nm technology node, which changed the MCU technology trend for automotive applications in performance, power, and reliability advantages. He led this development into market dominance to make a de-facto standard in MCU applications, which was followed by successful 40 nm and 28 nm SONOS-eFlash development. He has consistently led the MCU technology and business strategies enabling the world's No.1 MCU market share position by Renesas Electronics now, where he was responsible for R&D in all the embedded non -volatile memories and technology platforms for MCU products. He is now the Senior Vice-President and Chief Technology Officer at Renesas Electronics Corp. responsible for all the corporate R&D activities. He has authored and co-authored more than 60 journal papers and conference papers, as well as 293 US patents and 193 Japanese patents issued. He was a visiting scientist at the Media Laboratory, MIT, in 1987–88, and he has been a lecturer for a graduate course at the Tokyo Institute of Technology, Tokyo, in 2013–2015 Dr. Hidaka has served on program committees of technical conferences: ISSCC by the Memory Subcommittee Chair, Program Committee (ITPC) Vice-chair and Chair (2012), as well as A-SSCC, ICICDT, VLSI-TSA, IEICE-ICD, and ICDV. He is a member of the IEEE SSCS Adcom, an Associate Editor of JSSC, a Steering Committee member of Trans. VLSI Systems, an advisory board member for the IEEE SSCS Magazine, and Chair of IEEE-SSCS Kansai Chapter. He is an SSCS Distinguished Lecturer in 2015–2016

Prof. Makoto Ikeda (Tokio University)

Smart Image Sensors and applications to 3D range-finding

➔ **h**. *14.45 – 16.00* ➔

This lecture will highlight several 3-D range-finding techniques, including, high-speed 3-D range-finding techniques based on light-section method(1D projection), time-encoded pattern projection method(2D projection), lockin-pixel and SPAD techniques based on ToF. Followed by asics of each techniques, this lecture will cover both device structure optimized for each techniques, and circuits optimization to maximize their performance.

Makoto Ikeda received the BE, ME, and Ph.D. degrees in electrical engineering from the University of Tokyo, Tokyo, Japan, in 1991, 1993 and 1996, respectively. He joined the University of Tokyo as a research associate, in 1996, and now professor at the department of electrical engineering and information systems. At the same time he has been involving the activities of VDEC(VLSI Design and Education Center, the University of Tokyo), to promote VLSI design educations and researches in Japanese academia. He worked for asynchronous circuits design, smart image sensor for 3-D range finding, and time-domain circuits for associate memories. He has published more than 230 technical publications, including 10 invited papers, and 7 books/chapters. He has been serving various positions of various international conferences, including ISSCC IMMD sub-committee chair (ISSCC 2015 -), A-SSCC 2015 TPC Chair, VLSI Circuits Symposium PC Chair (will be for 2016/2017). He is a member of IEEE, IEICE Japan, IPSJ and ACM.